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## ***CS530x Schematic and Layout Guidelines***

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### **Introduction**

This document describes the schematic and layout guidelines for the CS5302P, CS5304P, CS5304S, CS5308P and CS5308S High Performance Multichannel Audio ADC.

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## 1 Recommended External Components

### 1.1 CS5302P Typical Connection Diagram

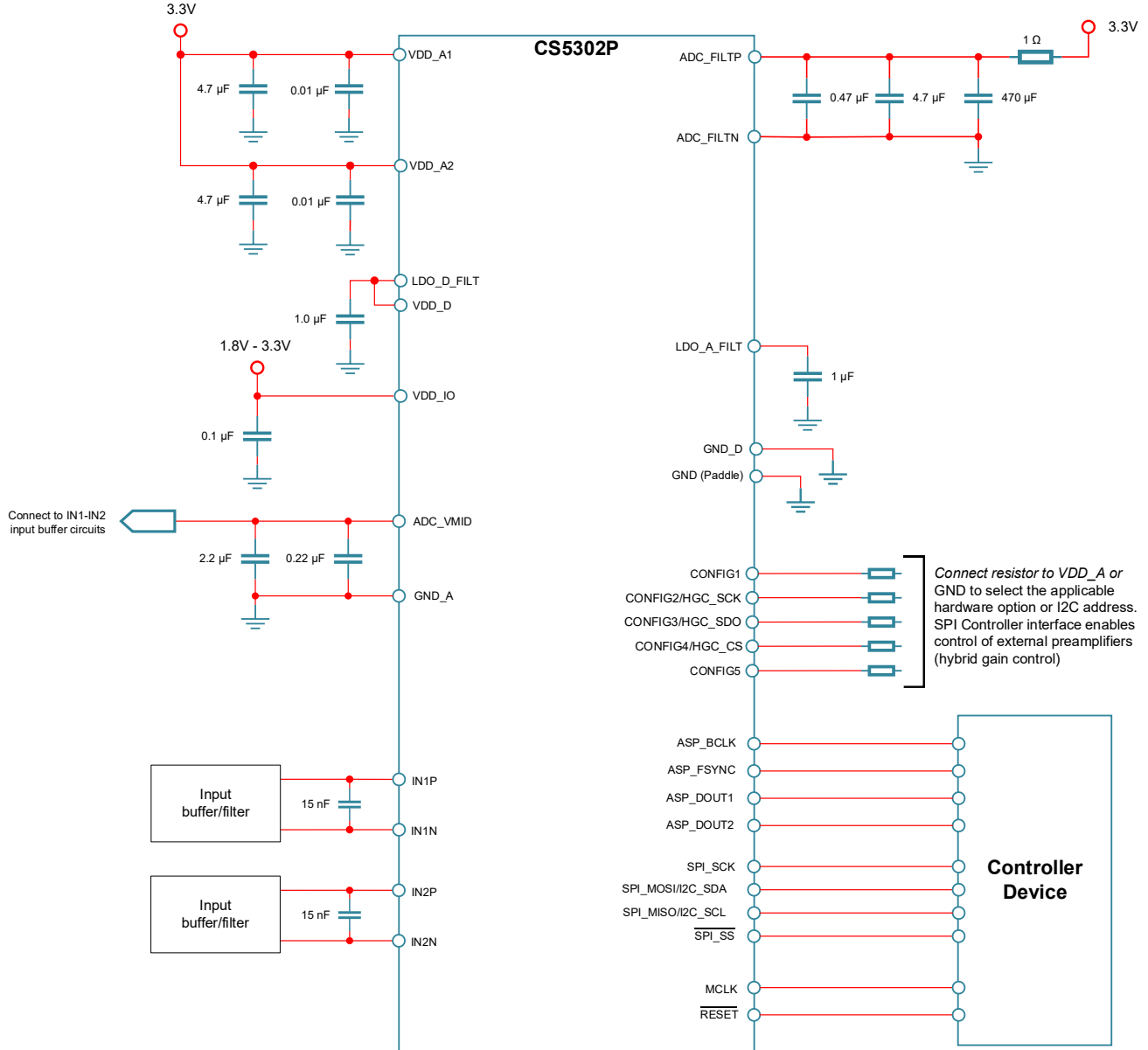


Figure 1: CS5302P Typical Connection

## 1.2 CS5304P/4S Typical Connection Diagram

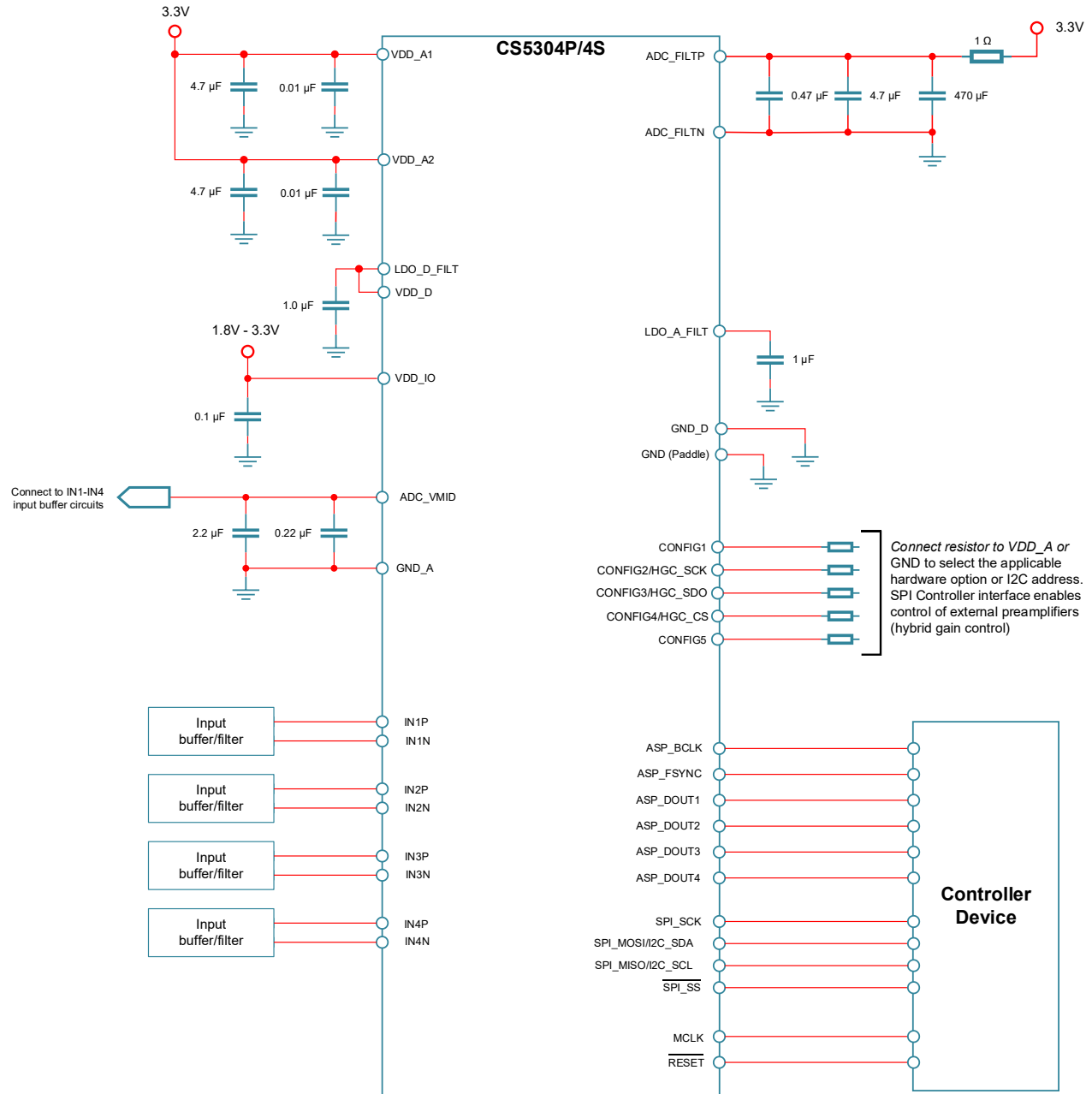


Figure 2: CS5304P/S Typical Connection

## 1.3 CS5308P/8S Typical Connection Diagram

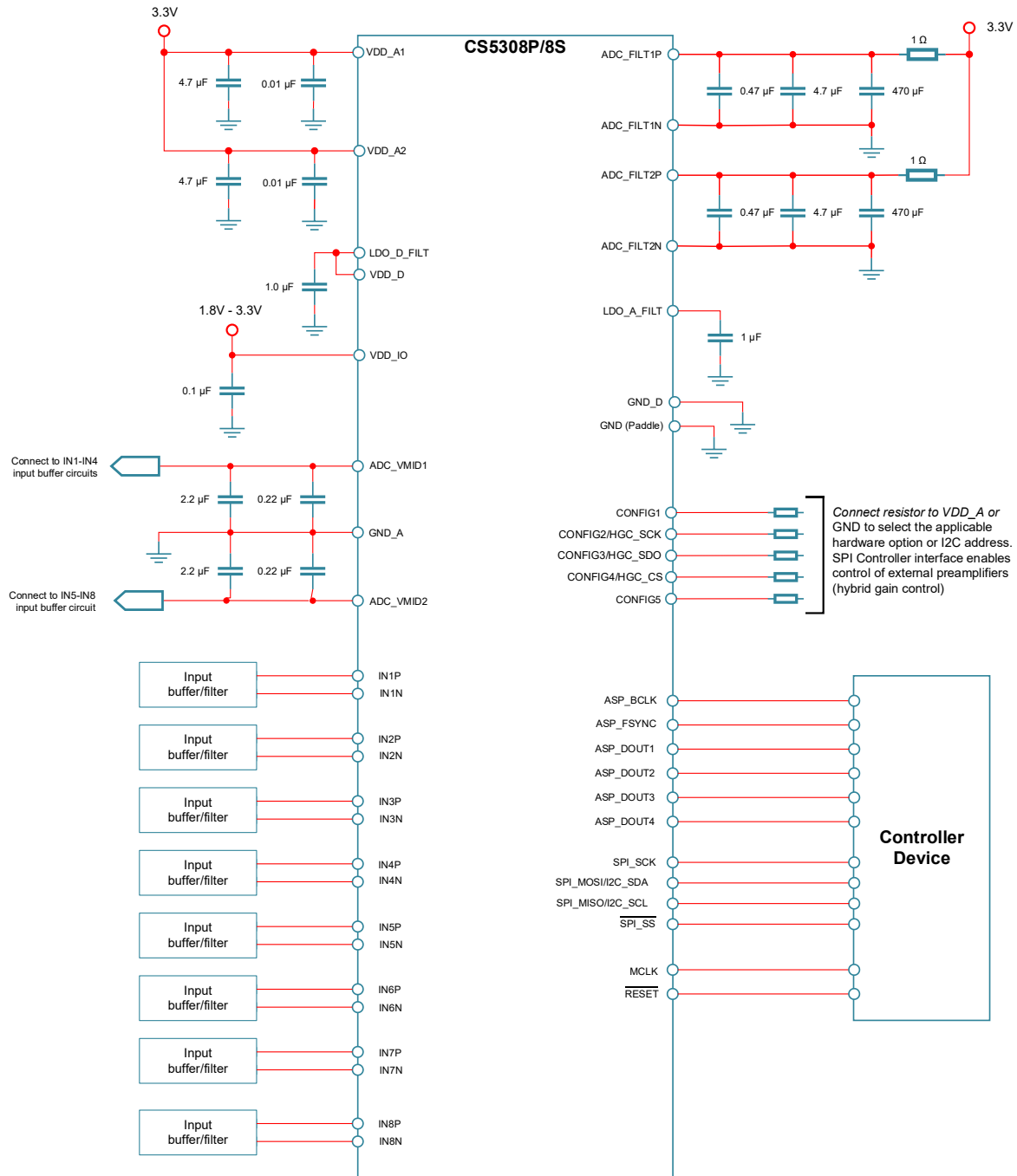


Figure 3: CS5308P/S Typical Connection

## 1.4 I2C Pull-Up

The I2C interface requires pull-up resistor to the VDD\_IO supply. The pull-up resistor value is determined by the following factors.

- Bus capacitance
- Minimum I2C drive strength of ICs on the I2C bus

Cirrus Logic recommends the I2C pull-up resistors should be between 2.2k $\Omega$  and 10k $\Omega$ .

**Table 1: i2c Pull-up Resistor**

|                       | Min | Typ         | Max | Units    |
|-----------------------|-----|-------------|-----|----------|
| I2C pull-up resistors |     | 2.2k to 10k |     | $\Omega$ |

## 1.5 Reset Pull-Up

An optional pull-up resistor to VDD\_IO (or pull-down to GND) is only required when the AP/MCU GPIO is unable to drive RESET at all times while CS5308P is powered.

## 1.6 LDO\_A\_FILT

The LDO\_A\_FILT decoupling capacitor must not de-rate to a value less than 0.8  $\mu$ F at 1.8V applied to it.

**Table 2: LDO\_A\_FILT Capacitor Derating**

| Capacitor Value | Derating Voltage | Min | Typ | Max | Units   |
|-----------------|------------------|-----|-----|-----|---------|
| 1.0 $\mu$ F     | 1.8V             | 0.8 |     |     | $\mu$ F |

## 1.7 LDO\_D\_FILT

The LDO\_D\_FILT decoupling capacitor must not de-rate to a value less than 0.8  $\mu$ F at 1.2V applied to it.

**Table 3: LDO\_D\_FILT Capacitor Derating**

| Capacitor Value | Derating Voltage | Min | Typ | Max | Units   |
|-----------------|------------------|-----|-----|-----|---------|
| 1.0 $\mu$ F     | 1.2V             | 0.8 |     |     | $\mu$ F |

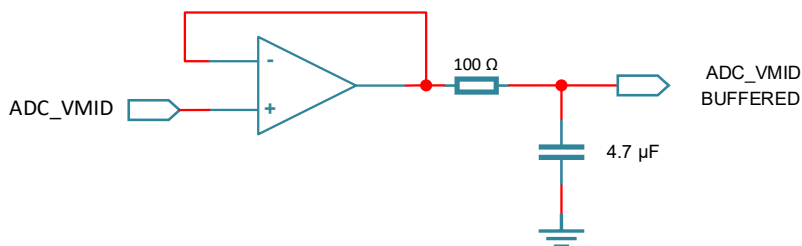
## 1.8 ADC\_VMID

The ADC\_VMID decoupling capacitors should not derate less than the minimum value shown in the table below:

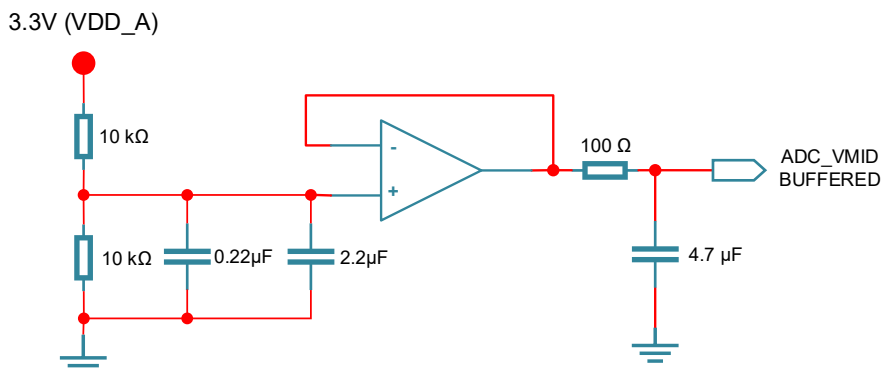
**Table 4: ADC\_VMID Capacitor Derating Specification**

| Capacitor Value    | Derating Voltage | Min | Typ | Max | Units         |
|--------------------|------------------|-----|-----|-----|---------------|
| 0.22 $\mu\text{F}$ | 1.65V            | 0.1 |     |     | $\mu\text{F}$ |
| 2.2 $\mu\text{F}$  | 1.65V            | 1.0 |     |     | $\mu\text{F}$ |

The VMID reference (common-mode level) for the input buffer can be provided from the ADC\_VMID output or a resistor divider circuit. If the total input bias current for the all the op-amps attached to ADC\_VMID is greater than 10 $\mu\text{A}$ , an external buffer is required to buffer the ADC\_VMID voltage, as shown in Figure 4.



**Figure 4 Example VMID Buffer Circuit**



**Figure 5 Example Resistor Divider ADC\_VMID Circuit**

## 1.9 ADC\_FILT

The ADC\_FILT decoupling capacitors should not derate less than the minimum value shown in the table below:

**Table 5: ADC\_FILT Capacitor Derating Specification**

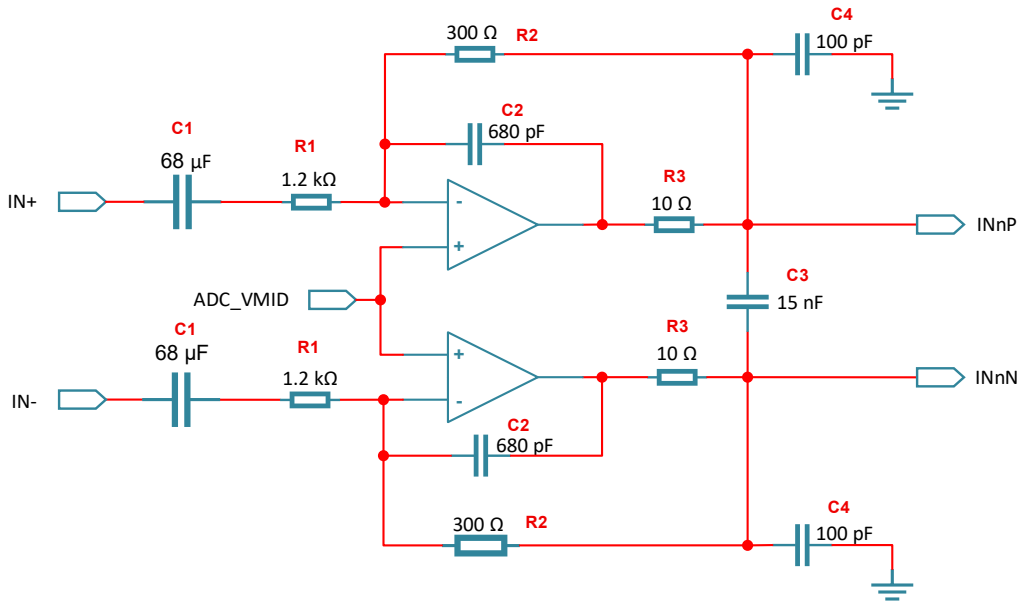
| Capacitor Value    | Derating Voltage | Min  | Typ | Max | Units         |
|--------------------|------------------|------|-----|-----|---------------|
| 0.47 $\mu\text{F}$ | 3.3V             | 0.22 |     |     | $\mu\text{F}$ |
| 4.7 $\mu\text{F}$  | 3.3V             | 2.2  |     |     | $\mu\text{F}$ |

The 470  $\mu\text{F}$  electrolytic decoupling capacitor on ADC\_FILT is a bulk capacitor for the ADC reference. The value of this capacitor can be reduced; however, this will increase the low frequency THD of the ADC.

## 1.10 Input Buffer Circuit

### 1.10.1 CS5302P Input Buffer Circuit

The analog input channels are supported using external buffer circuits. A typical buffer circuit is shown in Figure 6, comprising a high-pass filter and anti-alias filter. The typical buffer circuit shown produces a full-scale (0 dBFS) output from a 8 V<sub>RMS</sub> differential input.



**Figure 6: CS5302P Differential Input Buffer**

The high-pass filter is provided by the AC-coupling capacitor C1 and series resistor R1. Using the values shown, the –3 dB cut-off frequency ( $F_c$ ) can be calculated using the following equation:

$$F_c = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 1200 \times (68 \times 10^{-6})} = 1.95 \text{ Hz}$$

The anti-alias filter is provided by the op-amp and associated feedback components. The objective is to provide a flat passband for the audio input bandwidth, and sufficient attenuation at the ADC-modulator sample frequency. The low output impedance of the circuit minimizes the distortion of the signal path.

The typical filter shown provides a –3 dB cut-off frequency around 640 kHz, suitable for the highest CS5302P sample rate of 768 kHz. The attenuation slope of –12 dB/octave results in 42 dB attenuation at the ADC-modulator sample frequency of 6.144 MHz.

The –3 dB cut-off frequency is approximated by the following equation:

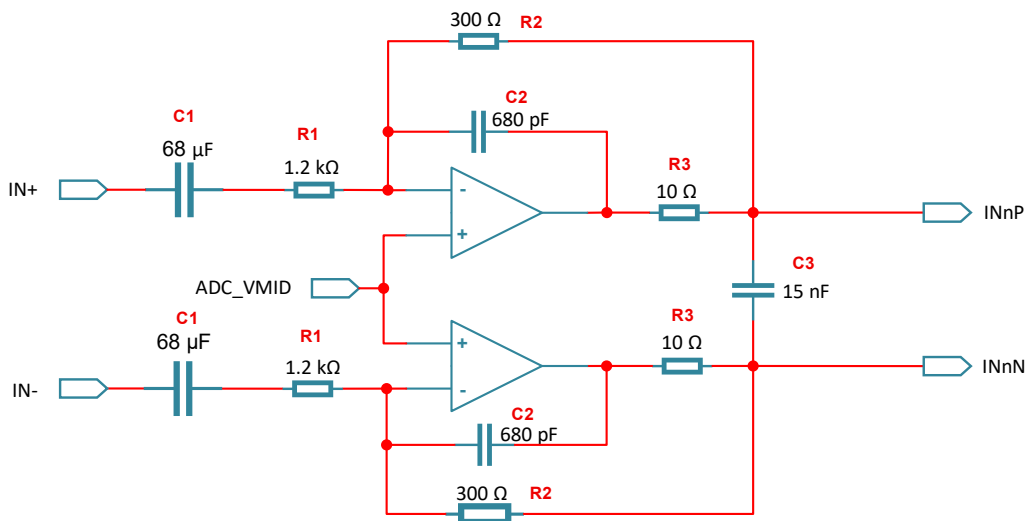
$$F_c = \frac{1}{2\pi \sqrt{R_2 R_3 C_2 2(C_3 + C_4)}} = \frac{1}{2\pi \sqrt{300 \times 10 \times 680 \times 10^{-12} \times 2 \times 15 \times 10^{-9}}} = 640 \text{ kHz}$$

The gain of the input buffer is determined by the ratio  $R1/R2$ . The gain should be configured to provide a full-scale signal of 2 V<sub>RMS</sub> at the input to the CS5302P. The values shown in Figure 6 provide a ratio of 4; in this configuration, the buffer supports a full-scale input of 8 V<sub>RMS</sub>.

The VMID reference (common-mode level) for the input buffer can be provided from the ADC\_VMID output. If the total input bias current for the all the op-amps attached to ADC\_VMID is greater than 10µA, an external buffer is required to buffer the ADC\_VMID voltage, as shown in **Figure 4**.

### 1.10.2 CS5304P/4S/8P/8S Input Buffer Circuit

The analog input channels are supported using external buffer circuits. A typical buffer circuit is shown in **Figure 7**, comprising a high-pass filter and anti-alias filter. The typical buffer circuit shown produces a full-scale (0 dBFS) output from a 8 V<sub>RMS</sub> differential input.



**Figure 7: CS5304P/4S/8P/8S Differential Input Buffer**

The high-pass filter is provided by the AC-coupling capacitor C1 and series resistor R1. Using the values shown, the –3 dB cut-off frequency ( $F_c$ ) can be calculated using the following equation:

$$F_c = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 1200 \times (68 \times 10^{-6})} = 1.95 \text{ Hz}$$

The anti-alias filter is provided by the op-amp and associated feedback components. The objective is to provide a flat passband for the audio input bandwidth, and sufficient attenuation at the ADC-modulator sample frequency. The low output impedance of the circuit minimizes the distortion of the signal path.

The typical filter shown provides a –3 dB cut-off frequency around 640 kHz, suitable for the highest CS5304P/4S/8P/8S sample rate of 768 kHz. The attenuation slope of –12 dB/octave results in 42 dB attenuation at the ADC-modulator sample frequency of 6.144 MHz.

The –3 dB cut-off frequency is approximated by the following equation:

$$F_c = \frac{1}{2\pi \sqrt{R_2 R_3 C_2 C_3}} = \frac{1}{2\pi \sqrt{300 \times 10 \times 680 \times 10^{-12} \times 2 \times 15 \times 10^{-9}}} = 640 \text{ kHz}$$

The gain of the input buffer is determined by the ratio  $R1/R2$ . The gain should be configured to provide a full-scale signal of 2 V<sub>RMS</sub> at the input to the CS5304P/4S/8P/8S. The values shown in **Figure 7** provide a ratio of 4; in this configuration, the buffer supports a full-scale input of 8 V<sub>RMS</sub>.

The VMID reference (common-mode level) for the input buffer can be provided from the ADC\_VMID output. If the total input bias current for the all the op-amps attached to ADC\_VMID is greater than 10µA, an external buffer is required to buffer the ADC\_VMID voltage, as shown in Figure 4.

### 1.10.3 Recommended Components

To achieve the specified performance characteristics, the choice of external components should observe the following recommendations:

- Capacitors should be stable dielectric types, such as C0G (NP0) or electrolytic.
- Resistors should be low value where possible, to minimize thermal noise.
- Low-noise op-amps should be used, such as Texas Instruments OP1656. The op-amps should meet the minimum performance requirements noted in Table 6

**Table 6 Op-Amp Specification**

| Parameter                    | Specification              |
|------------------------------|----------------------------|
| Input Noise                  | < 5 nV/ $\sqrt{\text{Hz}}$ |
| Unity Gain bandwidth (G = 1) | > 15 MHz                   |
| Slew Rate                    | 5 V/ $\mu\text{s}$         |
| THD+N                        | < -128 dB                  |

### 1.10.4 Unused Input Pins

The recommended input buffer circuit (see Figure 6 for CS5302P & Figure 7 for CS5304P/4S/8P/8S) provides a biased differential connection to the input pins INxP and INxN. Alternative input-buffer circuits may use only a single-ended connection to INxP or INxN. If a single-ended input configuration is used, the unused input pin must be connected to a buffered VMID reference. See Figure 4 and Figure 5 for a buffered VMID circuit. If one or more input channel is not used (disabled), the respective input pins INxP and INxN should be floating (no connection).

## 2 General Board Considerations

- Avoid routing digital signals between power planes on an adjacent layer.
- Avoid routing analogue and digital signals next to each other.
- If signals have to cross another signal on an adjacent layer, it is recommend having them cross perpendicular to prevent coupling.
- Signals must not cross power plane shapes and ground cut-offs on an adjacent layer.

## 3 Layout Guidelines

### 3.1 Note 1: Digital Signals

- Use controlled 50Ω characteristic impedance for digital signals.

### 3.2 Note 2: 33R Termination Resistors

- Place Termination resistor close to the device.

### 3.3 Note 3: Device Decoupling

- Place de-coupling capacitors close to the device.

### 3.4 Note 4: VMID Decoupling & GND\_A pins.

- Place de-coupling capacitors close to the device.
- Connect the GND for the VMID capacitors to ground at the closest GND\_A pin.
- The GND\_A pins should have their own connection to the ground plane and should not be directly connected to the GND paddle.

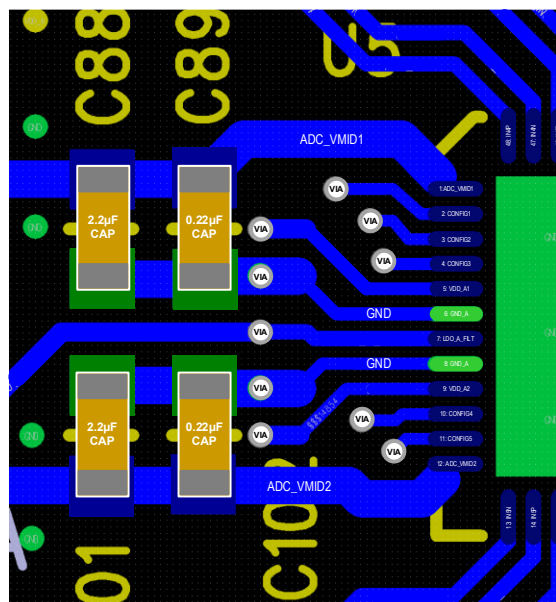


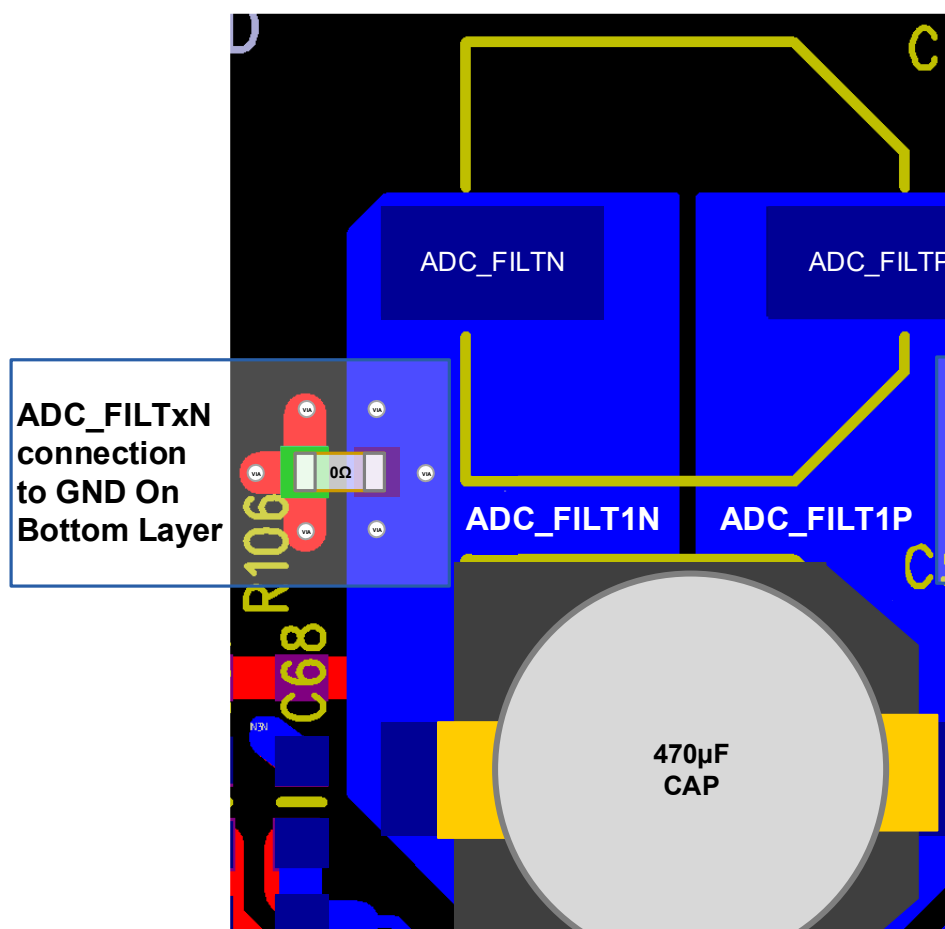
Figure 8: VMID Decoupling

### 3.5 Note 5: FILT Decoupling

- Place de-coupling capacitors close to the device.
- Place the resistor to ground for FILTxN after the 470uF capacitor.
- Place the resistor to VDD\_A for FILTxP after the 470uF capacitor.
- Order of priority for placement of capacitors

**Table 7: FILT Decoupling Placement Priority**

| Priority | Capacitor Value | Notes                          |
|----------|-----------------|--------------------------------|
| 1        | 0.47 $\mu$ F    |                                |
| 2        | 4.7 $\mu$ F     |                                |
| 3        | 470 $\mu$ F     |                                |
| 4        | 470 $\mu$ F     | Optional not fitted by default |



**Figure 9: FILT Decoupling**

## 3.6 Note 6: Input Buffer to ADC Input Pins Traces

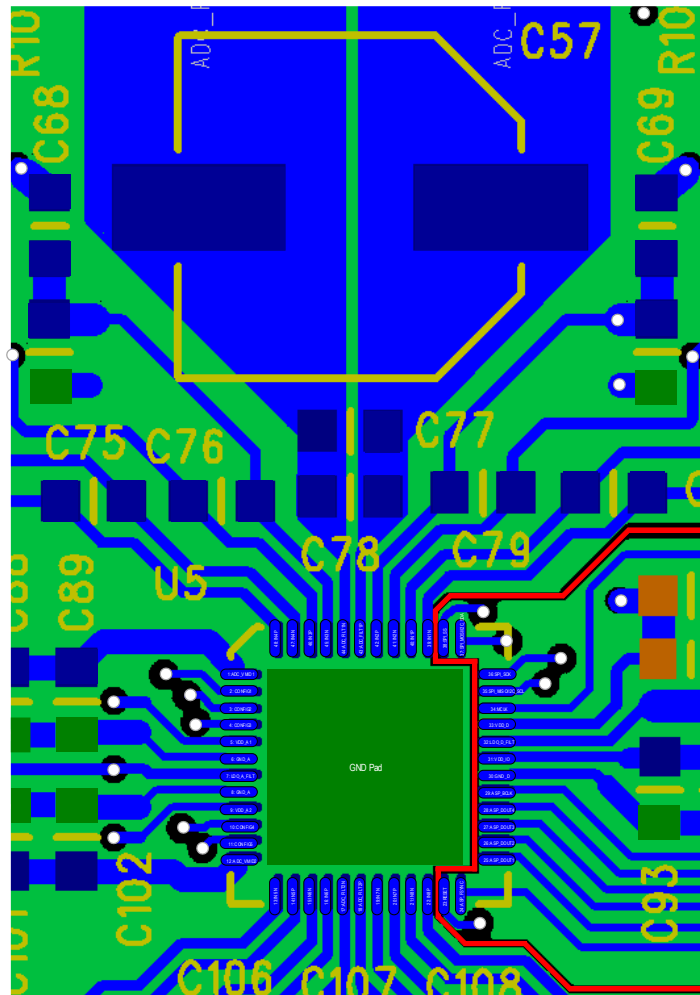
- To obtain best performance the DC resistance from the input buffer/filter to the ADC input pins should be as low as possible and not exceed 0.5Ω.
- (CS5302P Only)** The 15nF between ADC\_INxP/N should be placed as close as possible to the ADC input pins.
- The input signal traces should be routed as a pair with matched length.

**Table 8: Signal Track DC resistance for Best Performance**

|               | Min | Typ | Max | Units |
|---------------|-----|-----|-----|-------|
| DC Resistance |     |     | 0.5 | Ω     |

## 3.7 Note 7: Ground Cut out.

- The GND\_D pin should have its own connection to the ground plane and should not be directly connected to the GND paddle.
- There should be a ground cut-out to help isolate the noisy digital grounds and pins from the analog ground. The ground cutout should be deprecated on all ground layers.



**Figure 10: Ground Cut Out – Referenced to Top Layer of DC5308P-ADC Board**

## 4 Revision History

| Revision History |                                                                  |
|------------------|------------------------------------------------------------------|
| Revision         | Changes                                                          |
| 1.0<br>July 2025 | <ul style="list-style-type: none"><li>Initial version.</li></ul> |

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